APPENDIX A

GLOSSARY OF TELEPHONE SYSTEM ACRONYMS AND ABBREVIATIONS

A

ACO	Alarm Cut-Off
ADM	Add-Drop Multiplexer
ADTS	Automated Digital Terminal System
ADU	Alarm Display Unit
AIS	Alarm Indication Signal
AIU	Analog Interface Unit
ALIT	Automatic Loop Insulation Testing
AMI	Alternate Mark Inversion
ANSI	American National Standards Institute
AOW	Alarm & Order Wire
AOW	Alarm and Orderwire (Module)
AP	Application Processor
APM	Autonomous Protection Module
APS	Automatic Protection Switching
ASIC	Application-Specific Integrated Circuit
ASK	Amplitude-shift keyed
ASN	Abstract Syntax Notation
AUXS	Auxiliary Shelf

B

B8ZS	Bipolar with 8-Zero Substitution
BCP	Bank Control Processor
BER	Bit (or Boundary) Error Rate
BIP	Byte Interleaved Parity
BITS	Building Integrated Timing Supply
BOC	Bell Operating company
BPV	Bipolar Violations
BRA	Bite Rate Adapter or Bit Rate Access
BRI	Basic Rate Interface

C

CAD	Craft Access Device
CAS	Craft Access System
CAT	Craft Access Terminal
CES	Common Equipment Shelf
CEV	Controlled Environment Vault
CF	Coin First
CFU	Channel Fuse Unit
CHS	Channel Shelf
CID	Craft Interface Device
CLASS	Custom Local Area Signaling Service
CLEI	Common Language Equipment Identification (Bellcore)
CLF	Carrier Line Failure
CMIDU	Common Management Interface Data Unit
CNI	Calling Number Identification
CO	Central Office
CODEC	Coder/Decoder
Combo	Combination Codec and PCM filter
COP	AT&T provisioning OS
COT	Central office Terminal
CPE	Customer Premises Equipment
CPI	Calling Party Identification
CRC	Cyclic Redundancy Code
CSA	Customer (or Carrier) Service Area
CSC	Common Signaling Channel
CSMA	Collision Sense Multiple Access
CSP	Communication Strobe Card or Channel Shelf Processor
CTU	Channel Test Unit
CU	Channel Unit
CV	Coding Violation

D

DCC	Data Communications Channel
DCS	Digital Crossconnect System
DCU	Digital Connectivity Unit
DDS	Digital Data Service
DEU	DS1 Extension Unit
DID	Direct Inward Dial
DLC	Digital Loop Carrier
DM	Degraded Minutes
DS0	Digital Signal (Level) 0
DS-1	Digital Signal (Level) 1
DSX-1	Digital Signal Crossconnect (Level) 1
DTAU	Digital Test Access Unit
DTMF	Dual Tone Multi-Frequency
DTS	Digital Transmission System (Inc.)
DV	Data Valid

E

E1	European 32-channel PCM format
EOC	Embedded Operations Channel
ES	Errored Seconds
ESF	Extended Superframe Format
ESF/ndl	Extended Superframe Format with new data link
ESPOTS	Extended Special Plain Old Telephone Service

F

FAD	Fault (or Facility) Access Digroup
FCU	Fan control Unit
FDDI	Fiber Distributed Data Interface
FDL	Facility Data Link
FE	Far End
FEBE	Far End Block Error
FELB	Far End Loop Back
FELOF	Far End Loss Of customer data

FELP	Far End LooP back
FERF	Far End Receive Failure
FIFO	First In First Out
FITL	Fiber In The Loop
FPGA	Field Programmable Gate Array
F/O	Finer Optic

G

GS	Ground start

H

HDL	High Level Data Link
HDLC	High-level Data Link Control
HS	High speed

I

IDLC	Integrated Digital Loop Carrier
IDT	Integrated Digital Terminal
IMP	Integrated Multiprotocol Processor
INC	Incoming
IPL	Initial Program Load
ISDN	Integrated Services Digital Network
ISO	International Standardization Organization
ITS	Integrated Test System

J

K

L

LAN	Local Area Network
LAPx	Link Access Procedure on x (A, B, C, D) channel
LATA	Local Access and Transport Area
LBO	Line Build Out
LCCU	Low Cost Channel Unit
LDS	Local Digital Switch
LEC	Local Exchange Carrier
LFU	Line Fuse Unit

LIU Line Interface Unit
LMOS Loop Maintenance Operation System
LOF Loss of Frame
LOP Loss of Parity (or Pointer)
LOS Loss of Signal
LPTR Loop Test - Ring
LPTT Loop Test - Tip
LS Loop start
LSPM Low Speed Protection Module
LSSGR LATA Switching System Generic Requirements
LULT Line Unit Line Terminating (ISDN BRI)
LUNT Line Unit Network Terminating (ISDN BRI)

M

M13 DS1 to DS3 Multiplex
MAC Management and Control
MAU Maintenance Unit
MC Maintenance Center
MIB Management Information Base
MJ Major (Alarm)
MLT Mechanized Loop Test
MMU Memory Management Unit
MN Minor (Alarm)
MSB Most Significant Bit
MSDT Multi-Subscriber Distant Terminal
MSG Message line interface
MTAU Metallic Test Access Unit
MTS Message Telephone Service
MTTR Mean Time To Repair
MUX Multiplexer

N

NE Near End (or Network Element)
NEBS Network Equipment - Building System

NELB	Near End Loop Back
NELOF	Near End Loopback Of customer Data
NELP	Near End LooPback
NEP	Network Element Processor
NM	Network Management
NMA	Network Maintenance Alarm or Monitoring & Analysis System
NRZ	Non-Return to Zero logic
NSR	New Service Request (PSC-5 backplane signal)

O

OC	Optical Card
OC-12	Optical Channel (Level) 12
OC-3	Optical Channel (Level) 3
OCU	Office Channel Unit
OEI	Optical to Electrical Interface
OHT	On-hook Transmission
OIC	Optical Interface Card
OIM	Operations Interface Module
OOF	Out Of Frame
OPR	Optical Power Received
OPS/INE	Operations System/Intelligent Network Element
OPT	Optical Power Transmitted
OS	Operating (or Operations) System
OSI	Open System Interconnect
OSS	Operations Support System
OTDR	Optical Time-Domain Reflectometer
OTGR	Operations Technology Generic Requirements
OTS	Office Timing Supply
OVC	Output Verify Circuit
OW	Order Wire
O/E	Optical-to-Electrical conversion

P

PAL

PBX Private Branch Exchange
PCM Pulse code modulation
PCS Portable Communication System
PCU Power Converter or Control Unit
PGTC Pair Gain Test Controller
PLAR Private Line Automatic Ringdown
PLL Phase Locked Loop
PLM Phase Lock Multiplier
PM Performance Monitoring
PMN Power Minor Alarm
POC Pulse Operations Channel
POTS Plain Old Telephone Service
PPS Path Protection Switched
PRA Primary Rate Adapter (or Access)
PRI Primary Rate Interface (ISDN)
PSC Pulsecom
PSN Public Switched Network

Q

QBRICU Quad Basic Rate Interface Channel Unit
QCU Quad Channel Unit
QDS1 Quad DS-1

R

RBOC Regional Bell Operating Company
RDT Remote Digital Terminal
RMU Remote Measurement Unit
RSU Remote Switch Unit
RT(U) Remote Terminal (Unit)

S

SARTS Switched Access Remote Access System
SCP Signaling I/O Control Processor (FPGA)
SD Signal Degraded
SDEU Synchronous DS1 Extension Unit

SECC Secondary Error Correction Channel (DDS services)
SES Severely Errored Seconds
SF Super Frame (or Signal Failed)
SHR Self-Healing Ring
SLC Subscriber Loop Carrier (TM of AT&T)
SLIC Subscriber Loop Interface Circuit
SMDS Switched Multimegabit Data Service
SMT Surface Mount Technology
SOH Sonet OverHead
SONET Synchronous Optical Network
SOP SONET Overhead Processor (card)
SPE Synchronous Payload Envelope
SPOTS Special Plain Old Telephone Service
SS Supervisory System or System Services
STS1 Synchronous Transport Signal unit
STSM STS-1 Multiplexer
STSX Synchronous Transport Signal Extended

T

T1 Line-power DS1 to repeaters (1.544 Mbits/s)
T3 Standard transmission format at 45 Mbits/s
TAD Test Access Device (or Digroup)
TAN Test Access Network
TAP Test Access Path
TBD To Be Determined
TBOS Telemetry Byte-Oriented Serial (alarm reporting link)
TBSU Test Bus Segmentation Unit
TCA Threshold Crossing Alert
TCXO Temperature Controlled Crystal Oscillator
TDM Time division multiplex
TIRKS Test Inventory Record Keeping System
T-I/F ISDN "T" Interface
TL1 Transaction Language 1

	TMC	Time management Channel
	TRU	Transmit-receive Unit
	TSC	Test System Controller
	TSG	Timing Signal Generator
	TSI	Time Slot Interchange (or Interpolation)
U		
	U	ISDN "U" interface
	UART	Universal Asynchronous Receiver/Transmitter
	UAS	Un-Available Seconds
	UDLC	Universal Digital Loop Carrier
	UDT	Universal Digital Terminal
	UE	Underground Enclosure
	UVG	Universal Voice Grade
V		
	VCO	Voltage Controlled Oscillator
	VF	Voice frequency
	VRDT	Virtual Remote Digital Terminal
	VT	Virtual Tributary (Sonet term)
	VTG	Virtual Tributary Group (4 VT 1.5s)
W		
	WTR	Wait To Restore
X		
	XCT	Extended Test Controller
Y		
Z		
	ZBS	Zero Byte Supression

4.8.4. Registers

All of the processor registers are listed below starting from address FF. The odd addresses are not utilized and they are reserved for the internal RAM testing.

4.8.4.1. Register FE - Diagnostic Register

It provides the test software access into the ASIC without affecting the configuration of the ASIC. The microcontroller interface can be tested writing and reading back of this register.

4.8.4.2. Register FC - Interrupt Enable Register

The interrupt enable register, containing a mask bit per alarm register and a mask bit per interrupt vector outputs of the ASIC, allows to enable and disable the interrupts. A logic 1 level shall enable the interrupt. The register bits shall be set to 0 following Power_up.

Bit	Function	Type	Default
Bit 15	Mask of Alarm Reg. 13	R/W	0
Bit 14	Mask of Alarm Reg. 12	R/W	0
Bit 13	Mask of Alarm Reg. 11	R/W	0
Bit 12	Mask of Alarm Reg. 10	R/W	0
Bit 11	Mask of Alarm Reg. 9	R/W	0
Bit 10	Mask of Alarm Reg. 8	R/W	0
Bit 9	Mask of Alarm Reg. 7	R/W	0
Bit 8	Mask of Alarm Reg. 6	R/W	0
Bit 7	Mask of Alarm Reg. 5	R/W	0
Bit 6	Mask of Alarm Reg. 4	R/W	0
Bit 5	Mask of Alarm Reg. 3	R/W	0
Bit 4	Mask of Alarm Reg. 2	R/W	0
Bit 3	Mask of Alarm Reg. 1	R/W	0
Bit 2	Mask of Alarm Reg. 0	R/W	0
Bit 1	Mask of Secondary Int.	R/W	0
Bit 0	Mask of Primary Int.	R/W	0

4.8.4.3. Register FA - Interrupt Connect Register

The interrupt connect register allows to connect any alarm register interrupt to the primary or secondary interrupt lines of the ASIC. A logic 1 level shall connect the register to the primary, and a logic 0 shall connect the register to the secondary interrupt vector. The register bits are set to 0 following Power_up assigning all of the interrupts into the secondary interrupt.

Bit	Function	Type	Default
Bit 15	Connect Alm Reg. 13	R/W	0
Bit 14	Connect Alm Reg. 12	R/W	0
Bit 13	Connect Alm Reg. 11	R/W	0
Bit 12	Connect Alm Reg. 10	R/W	0
Bit 11	Connect Alarm Reg. 9	R/W	0
Bit 10	Connect Alarm Reg. 8	R/W	0
Bit 9	Connect Alarm Reg. 7	R/W	0
Bit 8	Connect Alarm Reg. 6	R/W	0
Bit 7	Connect Alarm Reg. 5	R/W	0
Bit 6	Connect Alarm Reg. 4	R/W	0
Bit 5	Connect Alarm Reg. 3	R/W	0
Bit 4	Connect Alarm Reg. 2	R/W	0
Bit 3	Connect Alarm Reg. 1	R/W	0
Bit 2	Connect Alarm Reg. 0	R/W	0
Bit 1-0	Unused	R	0

4.8.4.4. Register F8 - Interrupt Status Register

The interrupt register flags the processor on an activity in one of the alarm registers which was indicated by primary or secondary interrupt vectors. A logic 1 level shall reflect an activity in an alarm register regardless of the effect of the mask.

Bit	Function	Type	Default
Bit 15	Interrupt Alm Reg. 13	R	X
Bit 14	Interrupt Alm Reg. 12	R	X
Bit 13	Interrupt Alm Reg. 11	R	X
Bit 12	Interrupt Alm Reg. 10	R	X
Bit 11	Interrupt Alm Reg. 9	R	X
Bit 10	Interrupt Alm Reg. 8	R	X
Bit 9	Interrupt Alm Reg. 7	R	X
Bit 8	Interrupt Alm Reg. 6	R	X
Bit 7	Interrupt Alm Reg. 5	R	X
Bit 6	Interrupt Alm Reg. 4	R	X
Bit 5	Interrupt Alm Reg. 3	R	X
Bit 4	Interrupt Alm Reg. 2	R	X
Bit 3	Interrupt Alm Reg. 1	R	X
Bit 2	Interrupt Alm Reg. 0	R	X
Bit 1	Secondary Interrupt	R	X
Bit 0	Primary Interrupt	R	X

4.8.4.5. Register F6 - ASIC Revision Code & Configuration

The least significant 8 bit reflects the revision code of VTM ASIC which is currently defined as 02H.

The configuration pins of the ASIC are also included in the same register. Any change of the ABSEL or BUSMODE input pin is reflected into this register immediately.

Bit	Function	Type	Default
Bit 15-10	Unused	R	0
Bit 9	Busmode Pin (Config)	R	X
Bit 8	Absel Pin (Config)	R	X
Bit 7-0	ASIC Revision Code	R	02H

4.8.4.6. Register F4 - Global Control Register

ABSLICE : Provides the selection of a VT from A or B side. A logic 0 level shall indicate the mapping from A side, and a logic 1 from B side.

SYNSEL: Controls the multiplexer to select an 8kHz synchronization signal generated by one the four DS1 receive interface.

0 0 DS1 receive interface #0,
0 1 DS1 receive interface #1,
1 0 DS1 receive interface #2,
1 1 DS1 receive interface #3.

TREFSEL: Controls the multiplexer to select a 1.544 MHz reference clock generated by one of the four DS1 transmit interface.

0 0 DS1 transmit interface #0,
0 1 DS1 transmit interface #1,
1 0 DS1 transmit interface #2,
1 1 DS1 transmit interface #3.

DISPLOSS: Provides the mechanism to turn off the interrupts caused by P1P0 signaling multiframe indicator while dealing with asynchronous payload. A logic 1 level shall mask the interrupt caused by VT P1P0 Loss bit of the VT alarm register.

SYNEN: Controls the tristate driver of the 8kHz synchronization reference output SYN8K. A logic 0 shall force this output into tristate mode.

REFEN: Controls the tristate driver of the 1.544 MHz reference clock output TREFCK. A logic 0 shall force this output into tristate mode.

GASYN: Global Asynchronous VT flag. This should be set to logic 1 when at least one of the VT slices is carrying asynchronous VT payload. This will allow the OBINT bit of the Alarm Register F0 to be activated once every 500 usec.

Bit	Function	Type	Default
Bit 15	Unused	R/W	0
Bit 14	GASYN	R/W	0
Bit 13	REFEN	R/W	0
Bit 12	SYNEN	R/W	0
Bit 11	DISPLOSS - VT #4	R/W	0
Bit 10	DISPLOSS - VT #3	R/W	0
Bit 9	DISPLOSS - VT #2	R/W	0
Bit 8	DISPLOSS - VT #1	R/W	0
Bit 7-6	TREFSEL	R/W	0
Bit 5-4	SYNSEL	R/W	0
Bit 3	ABSLICE - #4	R/W	0
Bit 2	ABSLICE - #3	R/W	0
Bit 1	ABSLICE - #2	R/W	0
Bit 0	ABSLICE - #1	R/W	0

The register bits are set to 0 following Power_up.

4.8.4.7. Register F2 - Alarm Register 0

ALOSS: Clock loss detection of the CK19A clock input. The detection is performed using microcontroller clock MPCLK. A logic 1 shall indicate the error condition.

BLOSS: Clock loss detection of the CK19B clock input. The detection is performed using microcontroller clock MPCLK. A logic 1 shall indicate the error condition.

HWERR: The internal parity check mechanism of the ASIC which will flag the bad parts during normal operation. A logic 1 shall indicate the error condition.

Bit	Function	Type	Default
Bit 15-12	Unused	R	0
Bit 11	HWERR - TX B side	CL on RD	0
Bit 10	HWERR - TX A side	CL on RD	0
Bit 9	HWERR - Demap #4	CL on RD	0
Bit 8	HWERR - Map #4	CL on RD	0
Bit 7	HWERR - Demap #3	CL on RD	0
Bit 6	HWERR - Map #3	CL on RD	0
Bit 5	HWERR - Demap #2	CL on RD	0
Bit 4	HWERR - Map #2	CL on RD	0
Bit 3	HWERR - Demap #1	CL on RD	0
Bit 2	HWERR - Map #1	CL on RD	0
Bit 1	BLOSS	CL on RD	0
Bit 0	ALOSS	CL on RD	0

The register bits are set to 0 following Power_up and when they are read by software.

4.8.4.8. Register F0 - Alarm Register 1

SLMPINT: SLC-96 mode Mapper interrupt indicates the request for software read access into the ASIC, so a new 72 frame datalink information can be collected. A logic 1 indicates that the read buffer is full. This interrupt is only enabled if SLCEN bit (bit 11) of the mapper control register is set to logic 1.

SLDMINT: SLC-96 mode Demapper interrupt indicates the request for software write access into the ASIC, so a new 72 frame datalink information can be transmitted. A logic 1 indicates that the write buffer is empty. This interrupt is only enabled if SLCEN bit (bit 11) of the mapper control register is set to logic 1.

OBINT: O bit interrupt. It is generated once every 500 usec. A logic 1 indicates that the new O bits can be read and written. This interrupt is only enabled if GASYN bit (bit 14) of the global control register F4 is set to logic 1.

Bit	Function	Type	Default
Bit 15-9	Unused	R	0
Bit 8	OBINT	CL on RD	0
Bit 7	SLDMINT - DS1 #4	CL on RD	0
Bit 6	SLDMINT - DS1 #3	CL on RD	0
Bit 5	SLDMINT - DS1 #2	CL on RD	0
Bit 4	SLDMINT - DS1 #1	CL on RD	0
Bit 3	SLMPINT - DS1 #4	CL on RD	0
Bit 2	SLMPINT - DS1 #3	CL on RD	0
Bit 1	SLMPINT - DS1 #2	CL on RD	0
Bit 0	SLMPINT - DS1 #1	CL on RD	0

The register bits 0-8 are set to 0 following Power_up and when they are read by software.

4.8.4.9. Register EE - Alarm Register 2

H4_LOSS: The H4 tracking circuit generates an H4 loss signal based on the algorithm mentioned in the ASIC spec. A logic 1 shall indicate the error condition.

Bit	Function	Type	Default
Bit 15-1	Unused	R	0
Bit 0	A Side H4_LOSS	CL on RD	0

The register bit 0 is set to 0 following Power_up and when it is read by software.

4.8.4.10. Register EC - Alarm Register 3

VTAIS: A VT AIS register is included to monitor a VT AIS condition on both active and inactive receive bus interfaces to prevent switching into the inactive side while AIS is active. A logic 1 level alarm signal is generated detecting all ones in the V1 and V2, VT pointer bytes. The VT AIS indication shall be removed with a single 0 detected in the pointer bytes.

Bit	Function	Type	Default
Bit 15-4	Unused	R	0
Bit 3	VT AIS - VT #4	CL on RD	0
Bit 2	VT AIS - VT #3	CL on RD	0
Bit 1	VT AIS - VT #2	CL on RD	0
Bit 0	VT AIS - VT #1	CL on RD	0

The register bits 0-3 are set to 0 following Power_up and when they are read by software.

4.8.4.11. Register EA - Alarm Register 4

PE_INT: Bus failure is detected looking into the receive bus parity errors and decrementing a counter whose threshold is set by software. A transfer from count 1 to 0 shall set this register into the logic 1 level.

Bit	Function	Type	Default
Bit 15-1	Unused	R	0
Bit 0	A Side PE_INT	CL on RD	0

The register bit 0 is set to 0 following Power_up and when it is read by software.

4.8.4.12. Register E8 - Alarm Register 5

RP_RAMF: Reflected Parity Fifo full is generated whenever the 16 bit fifo is filled with the address of the tributaries containing parity errors. A logic 1 shall indicate the full condition of the FIFO.

Bit	Function	Type	Default
Bit 15-1	Unused	R	0
Bit 0	A Side RP_RAMF	CL on RD	0

The register bit 0 is set to 0 following Power_up and when it is read by software.

4.8.4.13. Register E6 - Alarm Register 6

Same as Register EE- Alarm Register 2, but it indicates the condition on B side.

4.8.4.14. Register E4 - Alarm Register 7

Same as Register EC- Alarm Register 3, but it indicates the condition on B side.

4.8.4.15. Register E2 - Alarm Register 8

Same as Register EA- Alarm Register 4, but it indicates the condition on B side.

4.8.4.16. Register E0 - Alarm Register 9

Same as Register E8- Alarm Register 5, but it indicates the condition on B side.

4.8.4.17. Register DE - Alarm Register 10

RVTPER: The parity error detected in the serial VT receive interface. A logic 1 shall indicate an odd parity error.

VTAIS: VT path AIS detected under the pointer interpretation rules. A logic 1 shall indicate the AIS condition.

VTLOP: VT Loss of pointer detected under the pointer interpretation rules. A logic 1 shall indicate the LOP condition.

PLOSS: P1P0 signaling multiframe loss. A logic 1 shall indicate the error condition.

YELLOW: VT path overhead V5 byte yellow bit. A set yellow bit shall set the register following ten multiframe filtering.

FERF: VT path overhead V5 byte ferf bit. A set ferf bit shall set the register following ten multiframe filtering.

LBLCHA: Any change VT path overhead V5 byte label bits shall set this register following five multiframe filtering. A logic 1 shall indicate that the LBL bits are new.

LABEL: VT path overhead V5 byte label bits. These three bits are filtered for five multiframes.

Bit	Function	Type	Default
Bit 15-10	Unused	R	0
Bit 9	RVTPER - VT #1	CL on RD	0
Bit 8	VTAIS - VT #1	CL on RD	0
Bit 7	VTLOP - VT #1	CL on RD	0
Bit 6	PLOSS - VT #1	CL on RD	0
Bit 5	YELLOW- VT #1	CL on RD	0
Bit 4	FERF - VT #1	CL on RD	0
Bit 3	LBLCHA - VT #1	CL on RD	0
Bit 2-0	LABEL - VT #1	RD	X

The register bits 3-9 are set to 0 following Power_up and when they are read by software.

4.8.4.18. Register DC - Alarm Register 11

Same as Register DE- Alarm Register 10, but it indicates the conditions on VT #2.

4.8.4.19. Register DA - Alarm Register 12

Same as Register DE- Alarm Register 10, but it indicates the conditions on VT #3.

4.8.4.20. Register D8 - Alarm Register 13

Same as Register DE- Alarm Register 10, but it indicates the conditions on VT #4.

4.8.4.21. Register D6 - RX Bus, VT Connect Register

VT1SEL: VT #1 Address in the STS-1. The addressing scheme is given below:

00000	No connection
00001	Tributary #1
00010	Tributary #2
00011	Tributary #3
00100	Tributary #4
00101	Tributary #5
00110	Tributary #6
00111	Tributary #7
01000	Tributary #8
01001	Tributary #9
01010	Tributary #10
01011	Tributary #11
01100	Tributary #12
01101	Tributary #13
01110	Tributary #14
01111	Tributary #15
10000	Tributary #16
10001	Tributary #17
10010	Tributary #18
10011	Tributary #19
10100	Tributary #20
10101	Tributary #21
10110	Tributary #22
10111	Tributary #23
11000	Tributary #24
11001	Tributary #25
11010	Tributary #26
11011	Tributary #27
11100	Tributary #28
11101	No connection
11110	No connection
11111	No connection

VT2SEL: VT #2 Address in the STS-1.

Bit	Function	Type	Default
Bit 15-10	Unused	R	0
Bit 9-5	VT1SEL	R/W	00H
Bit 4-0	VT2SEL	R/W	00H

The register bits shall be set to 0 following Power_up.

4.8.4.22. Register D4 - RX Bus, VT Connect Register

VT3SEL: VT #3 Address in the STS-1.
VT4SEL: VT #4 Address in the STS-1.

Bit	Function	Type	Default
Bit 15-10	Unused	R	0
Bit 9-5	VT3SEL	R/W	00H
Bit 4-0	VT4SEL	R/W	00H

The register bits shall be set to 0 following Power_up.

4.8.4.23. Register D2 - RX Bus, A Side Control Register

PTH_TH: Parity threshold is loaded in the 5 bit parity error down counter which will indicate the bus failure condition. The counter is decremented by one with each parity error until it reaches to zero.

LCL_LPBK: Local loopback connects the transmit bus output data and sync signals into the receive interface instead of the ones received from the ASIC pins. A logic 1 level shall indicate the loop condition.

STS_SEL: Provides the tracking on one of the three STS-1 payload. The selection scheme is given below:

0	0	STS-1 #1
0	1	STS-1 #2
1	0	STS-1 #3
1	1	Unused

Bit	Function	Type	Default
Bit 15-8	Unused	R	0
Bit 7-3	PTH_TH - A side	R/W	00H
Bit 2	LCL_LPBK - A side	R/W	0
Bit 1-0	STS_SEL - A side	R/W	00B

The register bits shall be set to 0 following Power_up.

4.8.4.24. Register D0 - RX Bus, B Side Control Register

Same as Register D2, but it provides the control signals on B side.

4.8.4.25. Register CE - Reflected Parity Check Control

The reflected parity error check can be enabled or disabled per VT. A logic 1 level shall enable the reflected parity error on a particular VT. This register contains the controls for VT #15-28. The register bits shall be set to 0 following Power_up.

Bit	Function	Type	Default
Bit 15-14	Unused	R	0
Bit 13	Enable check VT #28	R/W	0
Bit 12	Enable check VT #27	R/W	0
Bit 11	Enable check VT #26	R/W	0
Bit 10	Enable check VT #25	R/W	0
Bit 9	Enable check VT #24	R/W	0
Bit 8	Enable check VT #23	R/W	0
Bit 7	Enable check VT #22	R/W	0
Bit 6	Enable check VT #21	R/W	0
Bit 5	Enable check VT #20	R/W	0
Bit 4	Enable check VT #19	R/W	0
Bit 3	Enable check VT #18	R/W	0
Bit 2	Enable check VT #17	R/W	0
Bit 1	Enable check VT #16	R/W	0
Bit 0	Enable check VT #15	R/W	0

4.8.4.26. Register CC - Reflected Parity Check Control

Same as register CE, but it contains the controls for VT #1-14.
The register bits shall be set to 0 following Power_up.

Bit	Function	Type	Default
Bit 15-14	Unused	R	0
Bit 13	Enable check VT #14	R/W	0
Bit 12	Enable check VT #13	R/W	0
Bit 11	Enable check VT #12	R/W	0
Bit 10	Enable check VT #11	R/W	0
Bit 9	Enable check VT #10	R/W	0
Bit 8	Enable check VT #9	R/W	0
Bit 7	Enable check VT #8	R/W	0
Bit 6	Enable check VT #7	R/W	0
Bit 5	Enable check VT #6	R/W	0
Bit 4	Enable check VT #5	R/W	0
Bit 3	Enable check VT #4	R/W	0
Bit 2	Enable check VT #3	R/W	0
Bit 1	Enable check VT #2	R/W	0
Bit 0	Enable check VT #1	R/W	0

4.8.4.27. Register CA - TX Bus, VT Connect Register

Same as register D6, but it provides the connection for transmit bus.

4.8.4.28. Register C8 - TX Bus, VT Connect Register

Same as register D4, but it provides the connection for transmit bus.

4.8.4.29. Register C6 - TX Bus, A Side Control Register

FRCNT_EN: Enable test frame counter. The test frame counter generates the transmit bus synchronization signals from a free running counter as J1 is in fixed position (following C1). A logic 1 shall switch the control signals from this counter instead of the ones received in the bus interface.

RP_POLARITY: Reflected parity error polarity can be altered with this control bit.

H4_SRC: H4 synchronization select enables the interface to synchronize either with the H4 sync detected in the receive interface or C1J1V1 signal of the transmit bus interface. A logic 1 level shall connect the receive H4 multiframe and a logic 0 level shall connect the transmit V1 multiframe synchronization into the transmit bus interface.

H4_SEQ: The H4 sequence can be generated as long 3 msec, or short 500 usec. A logic 1 level shall enable the long sequence to be generated.

H4_INS: H4 byte is generated and inserted into the VT path overhead under the control of this register. A logic 1 shall insert the H4 byte into the STS-1 payload.

STS_SEL: Provides the tracking on one of the three STS-1 payload. The selection scheme is given below:

0	0	STS-1 #1
0	1	STS-1 #2
1	0	STS-1 #3
1	1	Unused

DLY_CTL: Delays the outputs of the tributary counter to match with the delays on the reflected parity path. The reflected parity error should be returned in the same STS-1 boundary which it was transmitted. The selection scheme is given below:

0	0	3 clock delay
0	1	6 clock delay
1	0	9 clock delay
1	1	12 clock delay

PE_INS: Creates parity errors on the outgoing data when it is set to logic 1.

VT_AIS: Inserts VT AIS per VT when it is set to logic 1. This feature has been added to be able to insert AIS on the outgoing data when the normal data is looped into the receive side.

Bit	Function	Type	Default
Bit 15-14	Unused	R	0
Bit 13	FRCNT_EN - A side	R/W	0
Bit 12	RP_POLARITY-A side	R/W	0
Bit 11	H4_SRC - A side	R/W	0
Bit 10	H4_SEQ - A side	R/W	0
Bit 9	H4_INS - A side	R/W	0
Bit 8-7	STS_SEL - A side	R/W	0
Bit 6-5	DLY_CTL - A side	R/W	0
Bit 4	PE_INS - A side	R/W	0
Bit 3	LoopAIS VT #4-A side	R/W	0
Bit 2	LoopAIS VT #3-A side	R/W	0
Bit 1	LoopAIS VT #2-A side	R/W	0
Bit 0	LoopAIS VT #1-A side	R/W	0

The register bits shall be set to 0 following Power_up.

4.8.4.30. Register C4 - TX Bus, B Side Control Register

Same as Register C6, but it provides the control signals on B side.

4.8.4.31. Register BE-A0 - A side Reflected Parity Registers

The tributary address of the reflected parity error are stored in a fifo. This fifo is directly accessible by microcontroller interface to read. Software access should be provided only when a fifo full interrupt is received.
The RAM shall not be cleared upon Power_up.

Bit	Function	Type	Default
Bit 15-5	Unused	R	0
Bit 4-0	VT Address - A side	R	X

4.8.4.32. Register 9E-80 - B side Reflected Parity Registers

Same as Registers BE-A0, but it contains the tributary addresses for B side.

4.8.4.33. Register 7E - Mapper Control DS1 #4

ESSEL: It provides the selection control for one of the two elastic store on the DS1 data path. It is used in the ASIC with the combination of the BUSMODE input signal, and ASYRX register bit which controls different mappings in the ASIC. ESSEL shall be effective for DS1 to byte synchronous floating VT mapping.
A logic 1 shall enable the Dual Bank RAM whose slips are in the frame boundaries.
A logic 0 shall enable the 16-byte elastic store generating VT pointer adjustments related to the offset of the received DS1 clock.

ASYRX: It enables the ASIC to map the DS1 into the floating asynchronous VT with bit stuffing. A logic 1 shall indicate asynchronous mapping.

LOOPDS1: Loops the transmit DS1 data, clock and multiframe synchronization signals into the receive interface.

SLCEN: It enables the ASIC to drop and add the SLC-96 frame data link. A logic 1 shall indicate the operation in the 72 frames SLC-96 mode.

CLRCHA: It provides robbed bit or clear channel signaling control per DS0. A logic 1 shall indicate the robbed bit signaling. Ch 17-24 are controlled by this register.

Bit	Function	Type	Default
Bit 15-12	Unused	R	0
Bit 11	SLCEN	R/W	0
Bit 10	LOOPDS1	R/W	0
Bit 9	ASYRX	R/W	0
Bit 8	ESSEL	R/W	0
Bit 7	CLRCHA- DS0 Ch24	R/W	0
Bit 6	CLRCHA- DS0 Ch23	R/W	0
Bit 5	CLRCHA- DS0 Ch22	R/W	0
Bit 4	CLRCHA- DS0 Ch21	R/W	0
Bit 3	CLRCHA- DS0 Ch20	R/W	0
Bit 2	CLRCHA- DS0 Ch19	R/W	0
Bit 1	CLRCHA- DS0 Ch18	R/W	0
Bit 0	CLRCHA- DS0 Ch17	R/W	0

The register bits shall be set to 0 following Power_up.

4.8.4.34. Register 7C - Mapper Control DS1 #4

It provides clear channel control bits for DS0 channels 1-16 for the DS1 #4..

Bit	Function	Type	Default
Bit 15	CLRCHA- DS0 Ch16	R/W	0
Bit 14	CLRCHA- DS0 Ch15	R/W	0
Bit 13	CLRCHA- DS0 Ch14	R/W	0
Bit 12	CLRCHA- DS0 Ch13	R/W	0
Bit 11	CLRCHA- DS0 Ch12	R/W	0
Bit 10	CLRCHA- DS0 Ch11	R/W	0
Bit 9	CLRCHA- DS0 Ch10	R/W	0
Bit 8	CLRCHA- DS0 Ch9	R/W	0
Bit 7	CLRCHA- DS0 Ch8	R/W	0
Bit 6	CLRCHA- DS0 Ch7	R/W	0
Bit 5	CLRCHA- DS0 Ch6	R/W	0
Bit 4	CLRCHA- DS0 Ch5	R/W	0
Bit 3	CLRCHA- DS0 Ch4	R/W	0
Bit 2	CLRCHA- DS0 Ch3	R/W	0
Bit 1	CLRCHA- DS0 Ch2	R/W	0
Bit 0	CLRCHA- DS0 Ch1	R/W	0

The register bits shall be set to 0 following Power_up.

4.8.4.35. Register 7A - SLC-96 Datalink Receive #4

SFLOSS: SLC-96 superframe loss. A logic 1 shall indicate that the datalink bits may not be correct.

M1 bit: SLC-96 frame bit received in the multiframe #5, frame 4. Each multiframe contains 12 frames and there are 6 multiframe in a 72 frame SLC-96 superframe.

M2 bit: SLC-96 frame bit received in the multiframe #5, frame 6.

M3 bit: SLC-96 frame bit received in the multiframe #5, frame 8.

A1 bit: SLC-96 frame bit received in the multiframe #5, frame 10.

A2 bit: SLC-96 frame bit received in the multiframe #5, frame 12.

S1 bit: SLC-96 frame bit received in the multiframe #6, frame 2.

S2 bit: SLC-96 frame bit received in the multiframe #6, frame 4.

S3 bit: SLC-96 frame bit received in the multiframe #6, frame 6.

S4 bit: SLC-96 frame bit received in the multiframe #6, frame 8.

Bit	Function	Type	Default
Bit 15	SFLOSS	CL on RD	0
Bit 14-9	Unused	R	0
Bit 8	M1 Bit	R	0
Bit 7	M2 Bit	R	0
Bit 6	M3 Bit	R	0
Bit 5	A1 Bit	R	0
Bit 4	A2 Bit	R	0
Bit 3	S1 Bit	R	0
Bit 2	S2 Bit	R	0
Bit 1	S3 Bit	R	0
Bit 0	S4 Bit	R	0

The register bits shall be set to 0 following Power_up.

4.8.4.36. Register 78 - SLC-96 Datalink Receive #4

C1 bit: SLC-96 frame bit received in the multiframe #2, frame 12.
C2 bit: SLC-96 frame bit received in the multiframe #3, frame 2.
C3 bit: SLC-96 frame bit received in the multiframe #3, frame 4.
C4 bit: SLC-96 frame bit received in the multiframe #3, frame 6.
C5 bit: SLC-96 frame bit received in the multiframe #3, frame 8.
C6 bit: SLC-96 frame bit received in the multiframe #3, frame 10.
C7 bit: SLC-96 frame bit received in the multiframe #3, frame 12.
C8 bit: SLC-96 frame bit received in the multiframe #4, frame 2.
C9 bit: SLC-96 frame bit received in the multiframe #4, frame 4.
C10 bit: SLC-96 frame bit received in the multiframe #4, frame 6.
C11 bit: SLC-96 frame bit received in the multiframe #4, frame 8.

Bit	Function	Type	Default
Bit 15-11	Unused	R	0
Bit 10	C1 Bit	R	0
Bit 9	C2 Bit	R	0
Bit 8	C3 Bit	R	0
Bit 7	C4 Bit	R	0
Bit 6	C5 Bit	R	0
Bit 5	C6 Bit	R	0
Bit 4	C7 Bit	R	0
Bit 3	C8 Bit	R	0
Bit 2	C9 Bit	R	0
Bit 1	C10 Bit	R	0
Bit 0	C11 Bit	R	0

The register bits shall be set to 0 following Power_up.

4.8.4.37. Register 76 - Mapper Control VT #4

LABEL: This register provides the LABEL bits of the V5 path overhead byte to be transmitted from the ASIC.
FERF: The content of this register is inserted into the V5 byte FERF bit position if hardware override option is not used.
FERFSEL: It provides the FERF selection from hardware or software source. A logic 1 shall enable the automatic FERF insertion by hardware.
YELLOW: The content of this register is inserted into the V5 byte YELLOW bit position.
SWAIS: It controls the insertion of VT path AIS in floating mode or UNICODE in the locked mode. A logic 1 shall generate the AIS.
DISAIS: It disables the automatic AIS insertion under hardware control. A logic 1 shall disable the AIS.
INVBIP2: The calculated BIP-2 parity bits are inverted to create the BIP-2 errors at the other end. A logic 1 shall invert both parity bits.
ASYNVT: Enables the ASIC to map the VT interface instead of the DS1. A logic 1 shall select the VT path between two ASICs.
LOOPVT: Provides the loopback in the serial VT interface. A logic 1 shall loop the serial VT outputs into the serial VT inputs.
TR8MD: This feature has been added to freeze the P1 P0 bits on 11 condition during UNICODE. A logic 1 shall indicate TR8 mode.

Bit	Function	Type	Default
Bit 15-12	Unused	R	0
Bit 11	TR8MD	R/W	0
Bit 10	LOOPVT	R/W	0
Bit 9	ASYNVT	R/W	0
Bit 8	INVBIP2	R/W	0
Bit 7	DISAIS	R/W	0
Bit 6	SWAIS	R/W	0
Bit 5	YELLOW	R/W	0
Bit 4	FERFSEL	R/W	0
Bit 3	FERF	R/W	0
Bit 2-0	LABEL	R/W	0

The register bits shall be set to 0 following Power_up.

4.8.4.38. Register 74 - Mapper Control VT #4

O bits of the asynchronous VT payload are inserted writing this register.

Bit	Function	Type	Default
Bit 15-8	Unused	R	0
Bit 7-4	O- BITS second FR	R/W	0H
Bit 3-0	O- BITS for third FR	R/W	0H

The register bits shall be set to 0 following Power_up.

4.8.4.39. Register 72 - Status Register Mapper & Demapper #4

SETDB: Indicates the slip condition of the Dual Bank data elastic store of the mapper. A logic 1 shall indicate a slip.

SETSIG: Indicates the slip condition of the Dual bank signaling elastic store of the mapper. A logic 1 shall indicate a slip.

DMSLIP: Demapper dsynchronizer elastic store slip indicator. A logic 1 shall indicate a slip.

Bit	Function	Type	Default
Bit 15-3	Unused	R	0
Bit 2	SETDB	CL on RD	0
Bit 1	SETSIG	CL on RD	0
Bit 0	DMSLIP	CL on RD	0

The register bits 0-2 are set to 0 following Power_up and when they are read by software.

4.8.4.40. Register 70 - Status Register Demapper #4

O bits of the asynchronous VT payload are received in this register.

Bit	Function	Type	Default
Bit 15-8	Unused	R	0
Bit 7-4	O- BITS second FR	R	0H
Bit 3-0	O- BITS for third FR	R	0H

The register bits shall be set to 0 following Power_up.

4.8.4.41. Register 6E - Demapper Control DS1 #4

DesynRef: Desynchronizer reference is switched from C1 SYNC into the J1 SYNC of the STS-1 payload. A logic 1 shall synchronize the interface with J1 sync.

DSDSP: It allows the ASIC to operate without a need for a DSP interface for locked mode mappings. A logic 1 shall disable the DSP control and the transmit DS1 clock shall be generated in a fixed sequence.

aisgen: A logic 1 shall generate DS1 AIS to be transmitted.

sigmode: The 12 or 24 frame multiframe signaling selection so the multiframe sync signal output is active once every 12 or 24 frames. A logic 0 indicates ESF and a logic 1 indicates SF.

mode: A logic 1 shall indicate the asynchronous DS1 mapping so the destuffing can be performed.

clkinv: DS1 clock can be inverted under software control. A logic 0 shall move the rising edge into the middle of the DS1 data (300nsec setup 300nsec hold) and a logic 1 level shall provide 50 nsec setup time and 600nsec hold respect to data.

DISAIS: A logic 1 level shall disable the AIS condition generated by hardware.

ccrb: It provides robbed bit or clear channel signaling control per DS0. A logic 1 shall indicate the robbed bit signaling. Ch 17-24 are controlled by this register.

Bit	Function	Type	Default
Bit 15	DISAIS	R/W	0
Bit 14	clkinv	R/W	0
Bit 13	mode	R/W	0
Bit 12	sigmode	R/W	0
Bit 11	aisgen	R/W	0
Bit 10	DSDSP	R/W	0
Bit 9	Unused	R/W	0
Bit 8	DesynRef	R/W	0
Bit 7	ccrb - DS0 Ch24	R/W	0
Bit 6	ccrb - DS0 Ch23	R/W	0
Bit 5	ccrb - DS0 Ch22	R/W	0
Bit 4	ccrb - DS0 Ch21	R/W	0
Bit 3	ccrb - DS0 Ch20	R/W	0
Bit 2	ccrb - DS0 Ch19	R/W	0
Bit 1	ccrb - DS0 Ch18	R/W	0
Bit 0	ccrb - DS0 Ch17	R/W	0

The register bits shall be set to 0 following Power_up.

4.8.4.42. Register 6C - Demapper Control DS1 #4

It provides clear channel control bits for DS0 channels 1-16 for the DS1 #4..

Bit	Function	Type	Default
Bit 15	ccrb - DS0 Ch16	R/W	0
Bit 14	ccrb - DS0 Ch15	R/W	0
Bit 13	ccrb - DS0 Ch14	R/W	0
Bit 12	ccrb - DS0 Ch13	R/W	0
Bit 11	ccrb - DS0 Ch12	R/W	0
Bit 10	ccrb - DS0 Ch11	R/W	0
Bit 9	ccrb - DS0 Ch10	R/W	0
Bit 8	ccrb - DS0 Ch9	R/W	0
Bit 7	ccrb - DS0 Ch8	R/W	0
Bit 6	ccrb - DS0 Ch7	R/W	0
Bit 5	ccrb - DS0 Ch6	R/W	0
Bit 4	ccrb - DS0 Ch5	R/W	0
Bit 3	ccrb - DS0 Ch4	R/W	0
Bit 2	ccrb - DS0 Ch3	R/W	0
Bit 1	ccrb - DS0 Ch2	R/W	0
Bit 0	ccrb - DS0 Ch1	R/W	0

The register bits shall be set to 0 following Power_up.

4.8.4.43. Register 6A - SLC-96 Datalink Transmit #4

M1 bit: SLC-96 frame bit transmitted in the multiframe #5, frame 4.
M2 bit: SLC-96 frame bit transmitted in the multiframe #5, frame 6.
M3 bit: SLC-96 frame bit transmitted in the multiframe #5, frame 8.
A1 bit: SLC-96 frame bit transmitted in the multiframe #5, frame 10.
A2 bit: SLC-96 frame bit transmitted in the multiframe #5, frame 12.
S1 bit: SLC-96 frame bit transmitted in the multiframe #6, frame 2.
S2 bit: SLC-96 frame bit transmitted in the multiframe #6, frame 4.
S3 bit: SLC-96 frame bit transmitted in the multiframe #6, frame 6.
S4 bit: SLC-96 frame bit transmitted in the multiframe #6, frame 8.

Bit	Function	Type	Default
Bit 15-9	Unused	R	0
Bit 8	M1 Bit	R/W	0
Bit 7	M2 Bit	R/W	0
Bit 6	M3 Bit	R/W	0
Bit 5	A1 Bit	R/W	0
Bit 4	A2 Bit	R/W	0
Bit 3	S1 Bit	R/W	0
Bit 2	S2 Bit	R/W	0
Bit 1	S3 Bit	R/W	0
Bit 0	S4 Bit	R/W	0

The register bits shall be set to 0 following Power_up.

4.8.4.44. Register 68 - SLC-96 Datalink Transmit #4

C1 bit: SLC-96 frame bit transmitted in the multiframe #2, frame 12.
C2 bit: SLC-96 frame bit transmitted in the multiframe #3, frame 2.
C3 bit: SLC-96 frame bit transmitted in the multiframe #3, frame 4.

C4 bit: SLC-96 frame bit transmitted in the multiframe #3, frame 6.
C5 bit: SLC-96 frame bit transmitted in the multiframe #3, frame 8.
C6 bit: SLC-96 frame bit transmitted in the multiframe #3, frame 10.
C7 bit: SLC-96 frame bit transmitted in the multiframe #3, frame 12.
C8 bit: SLC-96 frame bit transmitted in the multiframe #4, frame 2.
C9 bit: SLC-96 frame bit transmitted in the multiframe #4, frame 4.
C10 bit: SLC-96 frame bit transmitted in the multiframe #4, frame 6.
C11 bit: SLC-96 frame bit transmitted in the multiframe #4, frame 8.

Bit	Function	Type	Default
Bit 15-11	Unused	R	0
Bit 10	C1 Bit	R/W	0
Bit 9	C2 Bit	R/W	0
Bit 8	C3 Bit	R/W	0
Bit 7	C4 Bit	R/W	0
Bit 6	C5 Bit	R/W	0
Bit 5	C6 Bit	R/W	0
Bit 4	C7 Bit	R/W	0
Bit 3	C8 Bit	R/W	0
Bit 2	C9 Bit	R/W	0
Bit 1	C10 Bit	R/W	0
Bit 0	C11 Bit	R/W	0

The register bits shall be set to 0 following Power_up.

4.8.4.45. Register 66 - BIP-2 Error Accumulator VT #4

BIP-2 errors are accumulated for VT performance monitoring. The accumulator is accessible directly by software. The 12-bit value can accumulate maximum errors for 1.024 sec. The accumulator is an up counter which rolls to 0 from maximum count.

Bit	Function	Type	Default
Bit 15-12	Unused	R	0
Bit 11-0	BIP-2 Error Accum.	R	000H

The accumulator shall be set to 0 following Power_up.

4.8.4.46. Register 64 - FEBE Accumulator VT #4

Received FEBE bits are accumulated for VT performance monitoring. The accumulator is accessible directly by software. The 11-bit value can accumulate maximum FEBEs for 1.024 sec. The accumulator is an up counter which rolls to 0 from maximum count.

Bit	Function	Type	Default
Bit 15-11	Unused	R	0
Bit 10-0	FEBE Accumulator	R	000H

The accumulator shall be set to 0 following Power_up.

4.8.4.47. Register 62 - Positive Justification Accumulator VT #4

Received VT pointer increments are accumulated for VT performance monitoring. The accumulator is accessible directly by software. The 9-bit value can accumulate maximum pointer adjustments for 1.024 sec. The accumulator is an up counter which rolls to 0 from maximum count.

Bit	Function	Type	Default
Bit 15-9	Unused	R	0
Bit 8-0	PJ Accumulator	R	000H

The accumulator shall be set to 0 following Power_up.

4.8.4.48. Register 60 - Negative Justification Accumulator VT #4

Received VT pointer decrements are accumulated for VT performance monitoring. The accumulator is accessible directly by software. The 9-bit value can accumulate maximum pointer adjustments for 1.024 sec. The accumulator is an up counter which rolls to 0 from maximum count.

Bit	Function	Type	Default
Bit 15-9	Unused	R	0
Bit 8-0	NJ Accumulator	R	000H

The accumulator shall be set to 0 following Power_up.

4.8.4.49. Register 40-5E - VT Slice Registers #3

Same as explained in the registers 60-7E, but it contains the information for the DS1 and VT interface #3.

4.8.4.50. Register 20-3E - VT Slice Registers #2

Same as explained in the registers 60-7E, but it contains the information for the DS1 and VT interface #2.

4.8.4.51. Register 00-1E - VT Slice Registers #1

Same as explained in the registers 60-7E, but it contains the information for the DS1 and VT interface #1.

4.8.5. Timing between the Slice and Bus Interfaces

Each slice is capable of selecting the clock from either A side or B side. A latch has been included into the design for every signal transferred from the bus interface into the DS1 and VT slices or vice versa. These latches shall provide half a clock period hold time for every signal transferred between the blocks.

Figure 4-24 shows the signal flow from the transmit bus interface into the slice and Figure 4-25 shows the signal flow from the slice into the transmit bus interface.

The signal flow from the receive bus interface into the slice is shown in Figure 4-26.